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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/655,964
Filing Date: September 04, 2003
Appellant(s): COGDILL ET AL.

John P. Wagner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02 June 2009 appealing from the Office action mailed 1 December 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 06/02/2009 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,715,014	Johnson et al.	3-2004
5,583,449	Buuck	12-1996
5,111,080	Mizukami et al.	5-1992

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. (US 6,715,014).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Figure 3 of Johnson discloses a circuit for a memory module address bus comprising:

With respect to **claim 1**,

a transmission line (314) comprising a dampening impedance (324) between a driver (312) and a branch point (node between 318 and 320, hereinafter "star node") of said transmission line (314); and

a parallel termination impedance (326 – where 326 is parallel in reference to V_{TT} and star node) having one end coupled to said transmission line (314) between (see Figure 3b as shown above) said dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance (326) is on a same side of any memory module as said driver (where Figure 3b shows 326 and driving source below the memory modules);

said transmission line (314) having branches (316-322) from said branch point, wherein ones of said branches are coupled to at least one memory module interface (304).

With respect to **claim 2**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 3**,

Johnson teaches wherein said ones of said branches are coupled to two memory module interfaces (304, 306).

With respect to **claim 4**,

Johnson teaches wherein said ones of said branches are coupled to three memory module interfaces (302, 304 and 306).

With respect to **claim 5**,

Johnson teaches wherein said ones of said branches are coupled to four memory module interfaces (302, 304, 306 and 308).

With respect to **claim 7**,

Johnson teaches wherein said one end of said parallel termination impedance (end coupled to star node) is connected to said series dampening impedance (see Figure 3).

With respect to **claim 8**,

Figure 3 of Johnson discloses a circuit for reducing skew when addressing a memory module comprising:

a plurality of memory modules (302-308);

an address line (316-322) coupling said memory modules (302-308);

a transmission line (314) having a series dampening impedance (324) and a parallel termination impedance (326 – where 326 is parallel in reference to V_{TT} and star node) in a stub configuration, wherein said parallel termination impedance (326) is on a same side of any memory module as a driver (where Figure 3b shows 326 and driving source below the memory modules); and

said transmission line (314) having a first end coupled to a driver (312) and a second end connected at a point (star node) on said address line to reduce skew when addressing a memory module.

With respect to **claim 9**,

Johnson teaches wherein said second end of said transmission line is connected at substantially the midpoint of said address line (see Figure 3).

With respect to **claim 10**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 11**,

Johnson teaches wherein said parallel termination impedance (326) is connected to said series dampening impedance (324, see Figure 3).

With respect to **claim 12**,

Johnson teaches wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said address line at the middle memory module (Column 2, lines 24-39 and Figure 3).

With respect to **claim 13**,

Johnson teaches wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said address line at a point substantially midway between two memory modules closest to the mid-point of said address line (Column 2, lines 24-39 and Figure 3).

With respect to **claim 14**,

Figure 3 of Johnson discloses a system for addressing memory modules comprising:

a bus controller (inside 312);

a transmission line (314) comprising a series dampening impedance (324) between a driver (312) and a branch point (star node) of said transmission line; and

a parallel termination impedance (326 – where 326 is parallel in reference to V_{TT} and star node) having a first end coupled to said transmission line (314) between said series dampening impedance (324) and said branch point (star node) and a second end coupled to a termination voltage terminal (V_{TT}), wherein said parallel termination impedance (326) is on a same side of any memory module as a driver (where Figure 3b shows 326 and driving source below the memory modules);

said transmission line (314) having branches (316-322) from said branch point (star node), wherein ones of said branches are coupled to at least one memory module interface (304).

With respect to **claim 15**,

Johnson teaches wherein two branches (318, 320) of said branches from said branch point have substantially the same length (see Figure 3).

With respect to **claim 16**,

Johnson teaches wherein said transmission line is uni-directional (where the direction is from 312 to star node).

With respect to **claim 17**,

Johnson teaches wherein said ones of said branches (316) are coupled to two memory module interfaces (304 and 306).

With respect to **claim 18**,

Johnson teaches wherein said ones of said branches are coupled to three memory module interfaces (302, 304 and 306).

With respect to **claim 19**,

Johnson teaches wherein said ones of said branches are coupled to four memory module interfaces (302, 304, 306 and 308).

With respect to **claim 21**,

Johnson teaches wherein said first end of said parallel termination impedance (326) is connected to said series dampening impedance (324, at star node).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Buuck et al. (US 5,583,449).

With respect to **claim 6**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein the distance from said branch point to said one end of said parallel termination impedance is greater than the length of said branches.

Figure 2 of Buuck teaches a circuit for cancelling reflections on a transmission line that includes having the distance (L_1) between a branch point (80) and one of the devices (20 or 30) to be less than the overall distance between the driver and the device (sum of L_1 and L_2) for reducing electromagnetic interference (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the distances from a branch point to the end of the parallel termination impedance to be greater than the length of the branches as taught by Buuck to reduce electromagnetic interference (Abstract).

With respect to **claim 20**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein the distance from said branch point to said first end of said parallel termination impedance is greater than the length of said branches.

Figure 2 of Buuck teaches a circuit for cancelling reflections on a transmission line that includes having the distance (L_1) between a branch point (80) and one of the devices (20 or 30) to be less than the overall distance between the driver and the device (sum of L_1 and L_2) for reducing electromagnetic interference (Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the distances from a branch point to the end of the parallel termination impedance to be greater than the length of the branches as taught by Buuck to reduce electromagnetic interference (Abstract).

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Mizukami et al (US 5,111,080).

With respect to **claim 22**,

Figure 3 of Johnson discloses the circuit as claimed, but is silent to wherein said parallel impedance and said series impedance are mounted on opposite sides of a printed circuit board.

Figure 3 of Mizukami teaches a signal transmission circuit with impedance matching circuitry that includes a parallel impedance (R4) and a series impedance (R1) that are mounted on opposite sides (left and right sides) of a printed circuit board (Figure 3).

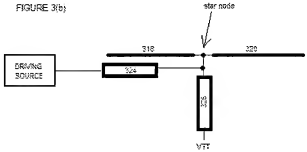
Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to mount resistors on opposite sides of the printed circuit board as taught by Mizukami because placement of resistors is a choice of design and there is no difference in terms of impedance matching or reduction of signal levels.

(10) Response to Argument

With respect to appellant's arguments on Page 9 that Johnson does not teach "... a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver", the Examiner respectfully disagrees.

The Examiner would like to note that the circuit as shown below (Figure 3b) is **equivalent** to the circuit shown in Figure 3 of Johnson. The Examiner would also like to add that it is irrelevant how these schematics are drawn as long as the connections/nodes are the same, since it is merely a matter of drawing choice.

As shown in Figure 3b (below), Johnson teaches "a parallel termination impedance (326) having one end coupled to said transmission line (shown as line connecting 326 to star node) between said series dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance is on the same side of any memory module as said driver (where 326 and driving source are below the memory modules). Therefore, the parallel termination impedance (326) is **between** the series dampening impedance (324) and the branch point (star node).



With respect to appellant's arguments on Page 10 that Johnson's Figure 3 shows "a parallel termination impedance 326 having one end coupled to a branch point, while the other end is coupled to a termination voltage", the Examiner respectfully disagrees and would again like to direct Appellant towards Figure 3b (as shown above). The circuit as shown above is equivalent to Johnson's Figure 3 and shows "a parallel termination impedance (326) having one end coupled to transmission line (shown as line connecting 326 to star node) between series dampening impedance (324) and branch point (star node).

With respect to appellant's arguments on Page 10 that "Johnson does not anticipate "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point,

wherein said parallel termination impedance is on the same side of any memory module as said driver", the Examiner respectfully disagrees and maintains the position as explained above.

With respect to the arguments directed towards claims 8 and 14 (one Page 10), the appellant relies on the arguments against the prior art and independent claim 1. The Examiner still respectfully disagrees with the appellant's arguments.

With respect to the arguments directed towards claims 2-5 and 7 depending on claim 1, claims 9-13 depending on claim 8, and claims 15-19 and 21 depending on claim 14, the appellant relies on the arguments against the prior art and independent claims 1, 8 and 14. The Examiner still respectfully disagrees with the appellant's arguments.

With respect to appellant's arguments on Page 12 that Johnson does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver", the Examiner respectfully disagrees. As shown in Figure 3b (above), Johnson teaches "a parallel termination impedance (326) having one end coupled to said transmission line (shown as line connecting 326 to star node) between said series dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance is on the same side of any memory module as said driver (where 326 and driving source are below the memory modules).

With respect to the arguments (directed towards claims 6 and 20) on Page 13 that Buuck does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver", the appellant relies on the arguments against the prior art reference of Johnson and independent claims 1 and 14. The Examiner would like to point out that primary reference Johnson teaches "a parallel termination impedance (326) having one end coupled to said transmission line (shown as line connecting 326 to star node) between said series dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance is on the same side of any memory module as said driver (where 326 and driving source are below the memory modules)".

With respect to appellant's arguments on Page 14 that Johnson does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver", the Examiner respectfully disagrees. As shown in Figure 3b (above), Johnson teaches "a parallel termination impedance (326) having one end coupled to said transmission line (shown as line connecting 326 to star node) between said series dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance is on the same side of any memory module as said driver (where 326 and driving source are below the memory modules).

With respect to the arguments (directed towards claim 22) on Page 14 that Mizukami does not teach "a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on the same side of any memory module as said driver", the appellant relies on the arguments against the prior art reference of Johnson and independent claims 1 and 14. The Examiner would like to point out that primary reference Johnson teaches "a parallel termination impedance (326) having one end coupled to said transmission line (shown as line connecting 326 to star node) between said series dampening impedance (324) and said branch point (star node), wherein said parallel termination impedance is on the same side of any memory module as said driver (where 326 and driving source are below the memory modules)".

Since the appellant's arguments with respect to claims 1, 8 and 14 are not persuasive, the rejection of claims depending from claims 1, 8 and 14 are maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Jany Tran/

Examiner, Art Unit 2819

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/Rexford N BARNIE/

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